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EXAMINER	
ZARNEKE, DAVID A	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/475,643	JASSOWSKI, MICHAEL A.	
	Examiner	Art Unit	
	David A. Zarneke	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-8,23-27 and 35-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-8,23-27 and 35-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments, filed 6/24/05, with respect to claims 1, 3, 5-8 and 23-27 have been fully considered but they are not persuasive.

Regarding the rejections over Hiraga, it is argued that the pads [5 & 6] are not staggered.

In response, it is clear in figures 1B and 3 that the pads [5 & 6] are staggered. They are obviously offset (staggered) from each other. Further, staggered pads are taught at column 3, lines 62+.

With respect to the rejections over Hayashi, two arguments are presented.

First, it is argued that the pads [39] are not staggered.

In response, it is clear in figure 10 that the pads [39] are staggered. They are obviously offset (staggered) from each other.

Second, it is argued that the pads [39] of Hayashi are arranged in two lines, not as an inner ring and an outer ring.

In response, when looking at figure 10, it is apparent that the two lines are arranged as an inner ring and an outer ring. Just because Hayashi doesn't use the same terminology to describe the invention doesn't mean that it can't refer to the same thing. Obviously, the two lines are arranged as an inner ring and an outer ring.

As to the rejections over Pendse, two arguments are presented.

First, it is argued that the pads [316] are not staggered.

In response, it is clear in figure 3 that the pads [316] are staggered. They are obviously offset (staggered) from each other.

Second, it is argued that the pads [316] are a pad ring, not as an inner ring and an outer ring.

In response, when looking at figure 3, it is apparent that the pad ring is actually an inner ring and an outer ring. Just because Pendse doesn't use the same terminology to describe the invention doesn't mean that it can't refer to the same thing. Obviously, the pad ring is arranged as an inner ring and an outer ring.

Applicant's arguments with respect to new claims 35-48 have been fully considered but they are not persuasive.

In re new independent claim 35, and its dependents 36-43, it is argued that the limitation that the conductive interconnects that couple the pre-driver cells to the driver cells are disposed on a layer other than the layer that the bond pads are disposed is not an obvious matter of design choice because it increases functionality.

The concept of placing interconnects underneath bond pads is more than well known in the art. This saves space on the chip surface and allows for more compact chips. Particularly in light of Hayashi's teaching that the chip can be in a multi-layer form that is connected by an interconnection layer between layers (6, 30+)

Regarding new independent claim 44, and its dependents 45-48, it is argued that the limitations of this claim distinguish over the cited references.

Note the rejection this claim and its dependents below.

Double Patenting

The terminal disclaimer filed 6/24/05 has been accepted and approved. Therefore, the double patenting rejection has been overcome.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 35 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 35 recites the limitation "the plurality of pre-driver cells" in line 10. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102(b)

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Hayashi et al., US Patent 5,581,109.

Hayashi (figures 1 & 10) teaches a semiconductor device, comprising:

a die [22] having a first edge and a core (figure 1 & 6, 5+);

a plurality of bond pads [39] configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads (figure 10);

a first plurality of driver cells [23] located between the first edge and the plurality of bond pads; and

a second plurality of driver cells [21] located between the plurality of bond pads and the core.

Claim 1 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Pendse et al., US Patent 5,818,114.

Pendse (figure 3) teaches a semiconductor device, comprising:

a die having a first edge and a core;

a plurality of bond pads [316] configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads (figure 3);

a first plurality of driver cells [314] located between the first edge and the plurality of bond pads; and

a second plurality of driver cells [312] located between the plurality of bond pads and the core.

Claim 44 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Pendse et al., US Patent 5,818,114.

Pendse (figure 3) teaches a semiconductor device, comprising:

a lead frame [abstract];

a die coupled to the lead frame, the die having

a first edge;

and a core;

a plurality of bond pads [316] configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads (figure 3);

a first plurality of driver cells [314] located between the first edge and the plurality of bond pads; and

a second plurality of driver cells [312] located between the plurality of bond pads and the core.

Claim Rejections - 35 USC § 102(e)

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 5, and 6 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Hiraga, US Patent 6,091,089.

Hiraga (figures 1A-1B & 3) teaches a semiconductor device, comprising:

a die [1] having a first edge and a core [2];

a plurality of bond pads [5 & 6] configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads (figures 1B & 3);

a first plurality of driver cells [10] located between the first edge and the plurality of bond pads; and

a second plurality of driver cells [4] located between the plurality of bond pads and the core.

With respect to claim 3, Hiraga teaches a plurality of pre-drive cells located between the second plurality of driver cells and the core (5, 20-40).

In re claim 5, Hiraga teaches a plurality of metal connections, each of the plurality of metal connections to couple one of the first and second pluralities of driver cells to one of the plurality of bond pads (4, 4-12).

Regarding claim 6, Hiraga teaches a plurality of conductive interconnects, each of the plurality of pre-driver cells coupled to one of the first and second pluralities of driver cells by at least one of the plurality of conductive interconnects (5, 20-40).

Claims 44, 45, 47 and 48 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Hiraga, US Patent 6,091,089.

Hiraga teaches a system comprising:

a lead frame (2, 45+);

a die [1] coupled to the lead frame, the die having

a first edge;

a core;

a plurality of bond pads [5 & 6] configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads (figures 1B & 3);

a first plurality of driver cells [10] located between the first edge and the plurality of bond pads; and

a second plurality of driver cells [4] located between the plurality of bond pads and the core.

With respect to claim 45, Hiraga teaches a plurality of pre-drive cells located between the second plurality of driver cells and the core (5, 20-40).

As to claim 47, Hiraga teaches each of the driver cells provides at least one of a drive strength, reception of incoming signals, and ESD protection of the core [column 4, lines 12+].

Regarding claim 48, Hiraga teaches each of the pre-drive cells provides communication between the core and one or more driver cells (4, 12+).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 3, 5-8 and 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al., US Patent 5,581,109, as applied to claim 1 above.

With respect to claim 3, though Hayashi fails to teach a plurality of pre-drive cells located between the second plurality of driver cells and the core, it would have been obvious to one of ordinary skill in the art at the time of the invention to a plurality of pre-drive cells because pre-drive cells are conventionally known in the art. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

In re claim 5, Hayashi teaches a plurality of metal connections [37a], each of the plurality of metal connections to couple one of the first and second pluralities of driver cells to one of the plurality of bond pads (figure 8).

Regarding claim 6, though Hayashi fails to teach a plurality of conductive interconnects, each of the plurality of pre-driver cells coupled to one of the first and second pluralities of driver cells by at least one of the plurality of conductive interconnects, it would have been obvious to one of ordinary skill in the art at the time of the invention to a plurality of conductive interconnects to couple the pre-driver cells to

the driver cells because this is conventionally known in the art. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

Regarding claim 7, though Hayashi fails to teach each of the plurality of conductive interconnects substantially more narrow in width than each of the plurality of metal connections, it would have been obvious to one of ordinary skill in the art at the time of the invention to optimize the relative widths of the conductive interconnects and the metal connects (MPEP 2144.05).

With respect to claim 8, though Hayashi fails to teach the first and second pluralities of driver cells each have a width of approximately 80 microns, it would have been obvious to one of ordinary skill in the art at the time of the invention to optimize the width of the first and second pluralities of driver cells (MPEP 2144.05).

In re claim 23, though Hayashi fails to teach each of the conductive interconnects coupling a pre-driver cell to one of the first and second driver cells has a width ranging from approximately 1 -2 microns, it would have been obvious to one of ordinary skill in the art at the time of the invention to optimize the width of the conductive interconnects (MPEP 2144.05).

Regarding claim 24, though Hayashi fails to teach wherein at least one pre-driver cell is coupled to one of the first and second driver cells via multiple conductive interconnects, the mere duplication of parts has no patentable significance unless a new and unexpected result is produced (In re Harza, 124 USPQ 378 (CCPA 1960))..

With respect to claim 25, though Hayashi fails to teach wherein at least one conductive interconnect is disposed on a layer other than a layer where the bond pads are disposed, the disposing of the conductive interconnect on a different layer is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)).

As to claim 26, though Hayashi fails to teach wherein at least one conductive interconnect is disposed on different layer underneath at least one bond pad, it is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)).

In re claim 27, though Hayashi fails to teach wherein at least one conductive interconnect is disposed on different layer underneath at least one driver cell, it is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)).

Claims 3, 5-8 and 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pendse et al., US Patent 5,818,114, as applied to claim 1 above.

With respect to claim 3, though Pendse fails to teach a plurality of pre-drive cells located between the second plurality of driver cells and the core, it would have been obvious to one of ordinary skill in the art at the time of the invention to a plurality of pre-drive cells because pre-drive cells are conventionally known in the art. The use of

conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

In re claim 5, Pendse teaches a plurality of metal connections [318a & 318b], each of the plurality of metal connections to couple one of the first and second pluralities of driver cells to one of the plurality of bond pads (figure 3).

Regarding claim 6, though Pendse fails to teach a plurality of conductive interconnects, each of the plurality of pre-driver cells coupled to one of the first and second pluralities of driver cells by at least one of the plurality of conductive interconnects, it would have been obvious to one of ordinary skill in the art at the time of the invention to a plurality of conductive interconnects to couple the pre-driver cells to the driver cells because this is conventionally known in the art. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

Regarding claim 7, though Pendse fails to teach each of the plurality of conductive interconnects substantially more narrow in width than each of the plurality of metal connections, it would have been obvious to one of ordinary skill in the art at the time of the invention to optimize the relative widths of the conductive interconnects and the metal connects (MPEP 2144.05).

With respect to claim 8, though Pendse fails to teach the first and second pluralities of driver cells each have a width of approximately 80 microns, it would have been obvious to one of ordinary skill in the art at the time of the invention to optimize the width of the first and second pluralities of driver cells (MPEP 2144.05).

In re claim 23, though Pendse fails to teach each of the conductive interconnects coupling a pre-driver cell to one of the first and second driver cells has a width ranging from approximately 1 -2 microns, it would have been obvious to one of ordinary skill in the art at the time of the invention to optimize the width of the conductive interconnects (MPEP 2144.05).

Regarding claim 24, though Pendse fails to teach wherein at least one pre-driver cell is coupled to one of the first and second driver cells via multiple conductive interconnects, the mere duplication of parts has no patentable significance unless a new and unexpected result is produced (In re Harza, 124 USPQ 378 (CCPA 1960))..

With respect to claim 25, though Pendse fails to teach wherein at least one conductive interconnect is disposed on a layer other than a layer where the bond pads are disposed, the disposing of the conductive interconnect on a different layer is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)).

As to claim 26, though Pendse fails to teach wherein at least one conductive interconnect is disposed on different layer underneath at least one bond pad, it is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)).

In re claim 27, though Pendse fails to teach wherein at least one conductive interconnect is disposed on different layer underneath at least one driver cell, it is an

obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)).

Claims 7, 8, and 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiraga, US Patent 6,091,089, as applied to claim 1 above.

Regarding claim 7, though Hiraga fails to teach each of the plurality of conductive interconnects substantially more narrow in width than each of the plurality of metal connections, it would have been obvious to one of ordinary skill in the art at the time of the invention to optimize the relative widths of the conductive interconnects and the metal connects (MPEP 2144.05).

With respect to claim 8, though Hiraga fails to teach the first and second pluralities of driver cells each have a width of approximately 80 microns, it would have been obvious to one of ordinary skill in the art at the time of the invention to optimize the width of the first and second pluralities of driver cells (MPEP 2144.05).

In re claim 23, though Hiraga fails to teach each of the conductive interconnects coupling a pre-driver cell to one of the first and second driver cells has a width ranging from approximately 1 -2 microns, it would have been obvious to one of ordinary skill in the art at the time of the invention to optimize the width of the conductive interconnects (MPEP 2144.05).

Regarding claim 24, though Hiraga fails to teach wherein at least one pre-driver cell is coupled to one of the first and second driver cells via multiple conductive

interconnects, the mere duplication of parts has no patentable significance unless a new and unexpected result is produced (In re Harza, 124 USPQ 378 (CCPA 1960))..

With respect to claim 25, though Hiraga fails to teach wherein at least one conductive interconnect is disposed on a layer other than a layer where the bond pads are disposed, the disposing of the conductive interconnect on a different layer is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)).

As to claim 26, though Hiraga fails to teach wherein at least one conductive interconnect is disposed on different layer underneath at least one bond pad, it is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)).

In re claim 27, though Hiraga fails to teach wherein at least one conductive interconnect is disposed on different layer underneath at least one driver cell, it is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)).

Claims 35-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al., US Patent 5,581,109.

Hayashi (figures 1 & 10) teaches a semiconductor device, comprising:

a die [22] having

a first edge, and

a core (figure 1 & 6, 5+);

a plurality of bond pads [39] configured in an array between the first edge and the core;

a first plurality of driver cells [23] located between the first edge and the plurality of bond pads; and

a second plurality of driver cells [21] located between the plurality of bond pads and the core.

Hayashi though fails to teach a plurality of conductive interconnects to couple each of the plurality of pre-driver cells to one of the first and second pluralities of driver cells, wherein at least one conductive interconnects is disposed on a layer other than a layer where the plurality of bond pads are disposed, it would have been obvious to one of ordinary skill in the art at the time of the invention to a plurality of pre-drive cells because pre-drive cells are conventionally known in the art. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07). especially in light of Hayashi's teaching that the chip can be in a multi-layer form with interconnections between each layer (6, 30+).

Regarding the limitation that conductive interconnects that couple the pre-driver cells to the driver cells are disposed on a layer other than the layer that the bond pads are disposed is merely an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)). The concept of placing interconnects underneath

bond pads is more than well known in the art. This saves space on the chip surface and allows for more compact chips.

With respect to claim 36, Hayashi teaches the plurality of bond pads are configured in a staggered array (figure 10).

As to claim 37, though Hayashi fails to teach a plurality of pre-drive cells located between the second plurality of driver cells and the core, it would have been obvious to one of ordinary skill in the art at the time of the invention to a plurality of pre-drive cells because pre-drive cells are conventionally known in the art. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

In re claim 38, Hayashi teaches the plurality of bond pads configured in the staggered array include an inner ring and an outer ring of bond pads (figure 10).

Regarding claim 39, Hayashi teaches a plurality of metal connections, each of the plurality of metal connections to couple one of the first and second pluralities of driver cells to one of the plurality of bond pads (figure 5 & 7, 60+).

With respect to claim 40, though Hayashi fails to teach each of the plurality of metal connections to couple one of the first and second driver cells to one of the bond pads has a width that is approximately up to 80 microns, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize the width of the metal connectors (MPEP 2144.05).

As to claim 41, Hayashi teaches each of the first driver cells is coupled to one of the outer ring of bond pads via one of the metal connections (figure 5).

In re claim 42, Hayashi teaches each of the second driver cells is coupled to one of the inner ring of bond pads via one of the metal connections (figure 5).

Regarding claim 43, though Hayashi fails to teach at least one metal connection coupling a bond pad and a driver cell has a width equivalent to a width of one of the respective bond pad and the driver cell, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize the relative width of the metal connectors (MPEP 2144.05).

Claims 35-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pendse et al., US Patent 5,818,114, in view of Hayashi et al., US Patent 5,581,109.

Pendse (figure 3) teaches a semiconductor device, comprising:

a die having

a first edge, and

a core;

a plurality of bond pads [316] configured in an array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads (figure 3);

a first plurality of driver cells [314] located between the first edge and the plurality of bond pads; and

a second plurality of driver cells [312] located between the plurality of bond pads and the core.

While Pendse fails to teach a plurality of conductive interconnects to couple each of the plurality of pre-driver cells to one of the first and second pluralities of driver cells,

wherein at least one conductive interconnects is disposed on a layer other than a layer where the plurality of bond pads are disposed, it would have been obvious to one of ordinary skill in the art at the time of the invention to a plurality of pre-drive cells because pre-drive cells are conventionally known in the art. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07). especially in light of Hayashi's teaching that the chip can be in a multi-layer form with interconnections between each layer (6, 30+).

Regarding the limitation that conductive interconnects that couple the pre-driver cells to the driver cells are disposed on a layer other than the layer that the bond pads are disposed is merely an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)). The concept of placing interconnects underneath bond pads is more than well known in the art. This saves space on the chip surface and allows for more compact chips.

Regarding claim 36, Pendse teaches the plurality of bond pads are configured in a staggered array (figure 3).

With respect to claim 37, though Pendse fails to teach a plurality of pre-drive cells located between the second plurality of driver cells and the core, it would have been obvious to one of ordinary skill in the art at the time of the invention to a plurality of pre-drive cells because pre-drive cells are conventionally known in the art. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

As to claim 38, Pendse teaches the plurality of bond pads configured in the staggered array include an inner ring and an outer ring of bond pads (figure 3).

In re claim 39, Pendse teaches a plurality of metal connections [318a & b], each of the plurality of metal connections to couple one of the first and second pluralities of driver cells to one of the plurality of bond pads.

Regarding claim 40, though Pendse fails to teach each of the plurality of metal connections to couple one of the first and second driver cells to one of the bond pads has a width that is approximately up to 80 microns, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize the metal connections width (MPEP 2144.05).

With respect to claim 41, Pendse teaches each of the first driver cells is coupled to one of the outer ring of bond pads via one of the metal connections (figure 3).

As to claim 42, Pendse teaches each of the second driver cells is coupled to one of the inner ring of bond pads via one of the metal connections.

In re claim 43, though Pendse fails to teach at least one metal connection coupling a bond pad and a driver cell has a width equivalent to a width of one of the respective bond pad and the driver cell, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize the relative metal connections width (MPEP 2144.05).

Claims 35-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiraga, US Patent 6,091,089, in view of Hayashi et al., US Patent 5,581,109.

Hiraga (figures 1A-1B & 3) teaches a semiconductor device, comprising:

a die [1] having

a first edge,

and a core [2];

a plurality of bond pads [5 & 6] configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads (figures 1B & 3);

a first plurality of driver cells [10] located between the first edge and the plurality of bond pads; and

a second plurality of driver cells [4] located between the plurality of bond pads and the core.

Hiraga, which teaches a plurality of conductive interconnects to couple each of the plurality of pre-driver cells to one of the first and second pluralities of driver cells (5, 20-40), fails to teach at least one conductive interconnects is disposed on a layer other than a layer where the plurality of bond pads are disposed.

Regarding the limitation that conductive interconnects that couple the pre-driver cells to the driver cells are disposed on a layer other than the layer that the bond pads are disposed is merely an obvious matter of design choice, especially in light of Hayashi's teaching that the chip can be in a multi-layer form with interconnections between each layer (6, 30+). Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)). The concept of placing interconnects underneath bond pads is more than well

known in the art. This saves space on the chip surface and allows for more compact chips.

Regarding claim 36, Hiraga teaches the plurality of bond pads are configured in a staggered array (figures 1B & 3).

With respect to claim 37, Hiraga teaches a plurality of pre-drive cells located between the second plurality of driver cells and the core (5, 20-40).

As to claim 38, Hiraga teaches the plurality of bond pads configured in the staggered array include an inner ring and an outer ring of bond pads (figures 1B & 3).

In re claim 39, Hiraga teaches a plurality of metal connections, each of the plurality of metal connections to couple one of the first and second pluralities of driver cells to one of the plurality of bond pads (4, 4-12).

Regarding claim 40, while Hiraga fails to teach each of the plurality of metal connections to couple one of the first and second driver cells to one of the bond pads has a width that is approximately up to 80 microns, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize the metal connections width (MPEP 2144.05).

With respect to claim 41, Hiraga teaches each of the first driver cells is coupled to one of the outer ring of bond pads via one of the metal connections (4, 4-12).

As to claim 42, Hiraga teaches each of the second driver cells is coupled to one of the inner ring of bond pads via one of the metal connections (4, 4-12).

In re claim 43, though Hiraga fails to teach at least one metal connection coupling a bond pad and a driver cell has a width equivalent to a width of one of the

respective bond pad and the driver cell, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize the relative metal connections width (MPEP 2144.05).

Claims 45-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pendse et al., US Patent 5,818,114, as applied to claim 44 above.

With respect to claim 45, though Pendse fails to teach a plurality of pre-drive cells located between the second plurality of driver cells and the core, it would have been obvious to one of ordinary skill in the art at the time of the invention to a plurality of pre-drive cells because pre-drive cells are conventionally known in the art. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

As to claim 46, Pendse teaches at least one of the first and second driver cells is a ESD (electrostatic discharge) cell (Figure 3, 314; [column 3, lines 50+]).

In re claim 47, Pendse teaches each of the driver cells provides at least one of a drive strength, reception of incoming signals, and ESD protection of the core [column 3, lines 50+].

Regarding claim 48, it would have been obvious to one of ordinary skill in the art at the time of the invention to use each of the pre-drive cells to provide communication between the core and one or more driver cells because this is inherently what pre-driver cells do, they provide communication between driver cells and the core.

Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hiraga, US Patent 6,091,089, as applied to claim 44 above, and further in view of Pendse et al., US Patent 5,818,114.

Hiraga fails to teach at least one of the first and second driver cells is a ESD (electrostatic discharge) cell.

Pendse teaches at least one of the first and second driver cells is a ESD (electrostatic discharge) cell (3, 50+).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the ESD driver cell of Pendse in the invention of Hiraga because ESD protection is important in chip and package structures to protect the chip.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication from the examiner should be directed to David A. Zarneke at (571)-272-1937. The examiner can normally be reached on M-F 7:30 AM-6 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Baumeister can be reached on (571)-272-1712. The fax phone number for the organization where this application is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David A. Zarneke
Primary Examiner
August 16, 2005